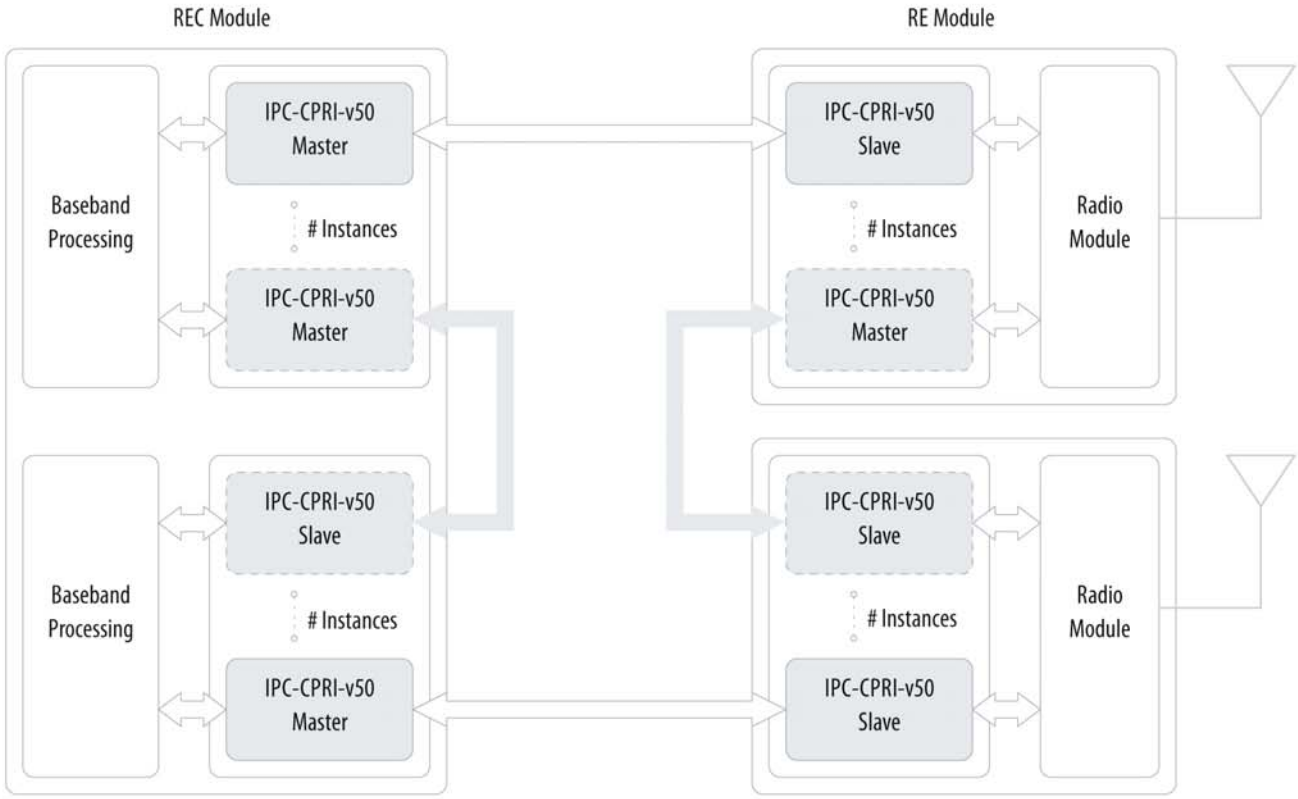
IPC-CPRI-v50 Product Brief

Product Overview

CPRI (Common Public Radio Interface) is an interfacing standard for high-speed communication of digital radio samples and control data between wireless infrastructure base station inter-modules. MTI's IPC-CPRI-v50 solution enables the quickest and most reliable deployment of REC (Radio Equipment Controller) and RE (Radio Equipment) interfaces. It includes all features required to support LTE/WCDMA/GSM/WiMAX wireless standards. MTI's IPC-CPRI-v50 is a self-contained and fully tested solution compliant with the latest CPRI v.5.0 specification. The IPC-CPRI-v50 is the market reference solution used today in many eNb field installations as well as in Tier1 DSP ASICs and FPGAs devices.



Key Features	Key Benefits
Multi-Standard Support	Enables individual or simultaneous operations for UTRA, E-UTRA, GSM & WiMAX standards.
High Performance	High Capacity operations with rates up to 9.8 Gbps and support for up to 64 AxC. Full compliance to ORI 1.0 and CMCC IR interface requirements.
Silicon Agnostic	Designed in VHDL-93 and targeting any RTL implementation like ASICs, ASSPs and FPGAs.
Fully Flexible and Future Proof	The design is modular and configurable. Support for full range sample widths (6 bits to 20 bits).
Enable low cost implementations	Leveraging clock rates at 1/40 of the baud rate, it enables low cost FPGA implementations.
Advanced Delay Measurement	Measurement resolutions below 1-ns in full compliance to CPRI v.5.0 for multi-hop apps.
Interoperability	Protocol interoperability guaranteed with most of the Tier1 and Tier2 OEM RE equipments on the field.

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Technical Specification

*Specifications are subject to change without prior notice

General*	Description and Availability			
Standards	CPRI v.5.0 [CPRI] and earlier			ORI v.1.0
Air Interfaces Supported	3GPP UTRA (UMTS WCDMA)	GSM-EDGE	3GPP E-UTRA (LTE)	IEEE 802.16 (WiMAX)
Applications and Technologies Supported	REC / RE		ASIC, ASSP, FPGA	VHDL-93 RTL
Line Baud Rates	From 614.4 Mbps up to 9.830 Gbps		Rate 1 to 7	Programmable
Master / Slave Mode	Yes			Programmable
Sample Widths	UMTS/GSM/LTE/WiMAX DL/UL	Option 1: 15/16 bits	Option 2: from 6 to 20 bits	Programmable
Mapping options	[CPRI] Section 4.2.7.2.3			Programmable
Mapping modes	[CPRI] Section 4.2.7.2.4 / 5 / 7			Programmable
Maximum Number of Data Carriers	64 AxC			Programmable
Low Latency Auxiliary Interface for Routing / Chaining	Yes		AUX Interface	
Start-up Sequence and Rate Auto-Negotiation	Yes		External via software (not included)	
Debug	Debug Diagnostic Loopbacks L1 / L2		Debug Signals	PRBS-23 Gen/Check
Transmitter*				
PCS (Delay Calibration, 8b10b encoder)	Yes		Optional	
Scrambling	Yes		Enabled for line rates > 3072 Gbps	
Receiver*				
PCS (Delay Measurment, 8b10b decoder)	Yes		Optional	
Scrambling	Yes		Rates > 3072 Gbps	
Delay Management*				
Receive delay measurement	Yes		Resolution >100 ps	[CPRI] R-19, R-20
Transmit delay calibration	Yes		40 bits shifter	[CPRI] R-20, R-21
Control and Management*				
Ethernet	Yes		Internal MAC	MII (Optional)
HDLC	Yes		Internal MAC	MII (Optional)
VSS	Yes		CPU or AUX Interface	
L1-Inband	Yes		CPU or AUX Interface	
Synchronization	Yes		CPU or AUX Interface	
Deliverables*				
Product Brief	Yes			
User Manual	Yes			
Verification Guide	Yes			
Regression Test Environment for Simulation	Yes		VHDL-93 RTL	portable
Test Cases, Test Report and Tools	Yes		Scripts, Mapping Config Tools and SW Drivers	
IPC Block	Encrypted RTL			portable
Resource Consumption	**Value**			
Total Logical gates*	~12,471 FF's (Option 1)			
Total Memory bits*	~54,370 bits (Option 1)		* Actual utlization may vary depending on configuration	
Interfaces	**Value**			
Shared memory IQ Carrier Interface	32 bits (Option 1)			
SERDES Interface (PHY not included)	10, 20 or 40 bits encoded		8, 16 or 32 bits unencoded	
CPU Interface	32-bits			
AUX Interface	32 bits + frame counters			
Ethernet / HDLC Interface	CPU Interface or external MII (Optional)			